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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/802,782	03/18/2004	Ryuji Imai	Q80544	5069

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EXAMINER	
LE, THAO X	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 07/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/802,782	IMAI ET AL.	
	Examiner	Art Unit	
	Thao X. Le	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 July 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) *26 and 27* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4/27/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of claims 1-25 in the reply filed on 05 July 2005 is acknowledged.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1, 4, 12, 15, 23, 25 are rejected under 35 U.S.C. 102(b) as being anticipated by US 6255899 to Bertin et al.

Regarding claims 1, 12 Bertin discloses an intermediate board in fig. 1A comprising: an intermediate board body 102 having first and second faces (top and bottom) wherein a semiconductor device 112 is to be mounted on at least one of said first and second faces, said semiconductor device 112 having a coefficient of thermal expansion that is equal to or larger than 2.0 ppm/^{0}C and smaller than 5.0 ppm/^{0}C, and having surface mount terminals 153a-n (or the bumps in fig. 1A), column 5 line 3, fig. 1C, said intermediate board body 102 having a plurality of through holes 108a-n, column 3 line 28, through which said first and second faces communicate with each other, fig. 1A, said intermediate board body 102 containing an inorganic insulating

material, column 3 line 16; and a plurality of conductor columns filling 108a-n, said through holes and containing a conductive metal, column 3 line 29, said conductor columns being to be connected with said surface mount terminals 153a-n.

Although the prior art does not specially disclose the claimed limitations 'semiconductor device 112 having a coefficient of thermal expansion that is equal to or larger than 2.0 ppm/^{0}C and smaller than 5:0 ppm/0C', this feature is seen to be inherently teaching because the microprocessor 112 of Bertin is made of silicon material, column 3 line 40; thus silicon material would have the thermal expansion equal to or larger than 2.0 ppm/^{0}C and smaller than 5:0 ppm/^{0}C, see Spielberger (6657134 in column 1 line30, Coyle (6753616) in column 5 line 12.

Regarding claims 4, 15, Bertin discloses the intermediate board wherein a metallization layer 108a-n is formed on an inner wall of each of said through holes, fig. 1A.

Regarding claim 23, Bertin discloses a substrate board with an intermediate board in fig. 1C, comprising: a substrate board 142, column 4 line 62, having a coefficient of thermal expansion that is equal to or larger than 5.0 ppm/^{0}C (alumina), column 3 lines 16-17 and having surface mount pads154a-n, column 5 line10; and an intermediate board 140, column 4 line 55 having: an intermediate board body 140 having a first face and a second face (top and bottom) which is mounted on a surface of said substrate board 142, fig. 1C, said intermediate board body 140 having a plurality of through holes 141 a-n, column 4 lines57-58, through which said first and second faces communicate with each other, fig. 1C, said intermediate board body 140

containing an inorganic insulating material, column 4 line 64; and a plurality of conductor columns 141 a-n filling said through holes and containing a conductive metal, column 4 line 58, said conductor columns being connected with said surface mount pads 154 a-n, fig. 1C.

Regarding claim 25, Bertin discloses a structural member in fig. 1C comprising: a semiconductor device 146 having a coefficient of thermal expansion that is equal to or larger than 2.0 ppm/^{0}C and smaller than 5.0/^{0}C and having surface mount terminals 150 a-n; a substrate board 142 having a coefficient of thermal expansion that is equal to or larger than 5.0 ppm/^{0}C, column 3 line 17, and having surface mount pads 154 a-n; and an intermediate board 140 having: an intermediate board body 140 having a first face (top face) on which said semiconductor device 146 is mounted, having a second face (bottom) which is mounted on a surface of said substrate board 142, fig. 1C, and having a plurality of through holes 141 a-n through which said first and second faces communicate with each other, said intermediate board body 140 containing an inorganic insulating material, column 3 line 16; and a plurality of conductor columns 141 a-n filling said through holes and containing a conductive metal, column3 line 30, said conductor columns being connected with said surface mount terminals 150a-n and said surface mount pads 154 a-n, fig. 1C.

With respect to CTE of semiconductor chip, see discussion in the above claims 1 and 12.

4. Claims 3, 5, 9-10, 14, 16, 20-21 are rejected under 35 U.S.C. 102(b) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over US 6255899 to Bertin et al.

Regarding claims 3, 5, 14, 16, Bertin discloses the intermediate board according to claim 1, wherein said inorganic insulating material 102 is low-temperature firing ceramic, column 3 line 15, and said conductive metal 108a-n is at least one of copper and silver, column 3 line 30, wherein the metallization layer 108a-n is formed on an inner wall of each of said through holes, fig. 1A,

The process limitations "low-temperature firing" in claim 3 or "can not be fired simultaneously with a metal" in claim 5 do not carry weight in a claim drawn to structure. In re Thorpe, 277 USPQ 964 (Fed. Cir. 1985).

Regarding claim 9-10, 20-21, Bertin discloses the intermediate board wherein said intermediate board body 102 is made of a material, which is higher in rigidity than at least silicon, wherein said intermediate board body 102 is made of a material having a Young's modulus of 100 Gpa or higher.

Although the prior art does not specially disclose the claimed limitations 'higher in rigidity than at least silicon, wherein said intermediate board body 102 is made of a material having a Young's modulus of 100 Gpa or higher', this feature is seen to be inherently teaching because Bertin discloses the intermediate board 102 and semiconductor device 112 are made of alumina and silicon, respectively, that is substantially identical to that of the claimed materials; therefore these materials would have the same properties.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

7. Claims 2, 6-7, 11,13, 17-18, 22, 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 6255899 to Bertin et al. in view of US 5714800 to Thompson.

Regarding claim 2, 13, Bertin discloses the intermediate board wherein said through holes 108a-n have a diameter which is equal to or smaller than 125 μm, see fig. 6 and column 3 line 63-67 of US 6222276 (or Application 09/056,277 incorporated by reference as disclosed by Bertin (6,25,899) in column 3 line 38).

But Bertin does not disclose a minimum center-to-center distance between adjacent ones of said through holes is equal to or smaller than 250 μm.

However, Bertin does not disclose a minimum center-to-center distance between adjacent ones of said through holes108a-n, fig. 1A-C, has a general distance. Accordingly, it would have been obvious to one of ordinary skill in art to use through holes spacing teaching of Bertin in the range as claimed, because it has been held that where the general conditions of the claims are discloses in the prior art, it is not inventive to discover the optimum or workable range by routine experimentation. See In re Aller, 220 F.2d 454, 105 USPQ 233, 235 (CCPA 1955).

Regarding claims 6-7, 17-18, Bertin discloses the intermediate board wherein said intermediate board body 102 is made of alumina, column 3 line 16.

But Bertin does not disclose the thickness of said intermediate board body is 0.1 to 0.8 mm, or wherein said intermediate board body is made of silicon nitride, and a thickness of said intermediate board body is 0.1 to 0.7 mm.

However, Bertin discloses the thickness of said intermediate board body is about 5 mm, column 3 line 20. Accordingly, it would have been obvious to one of ordinary skill in art to use thickness teaching of Bertin in the range as claimed, because it has been held that where the general conditions of the claims are discloses in the prior art, it is not inventive to discover the optimum or workable range by routine experimentation. See In re Aller, 220 F.2d 454, 105 USPQ 233, 235 (CCPA 1955).

With respect to interposer is made of silicon nitride, Thompson discloses a interposer can be made of organic or inorganic materials including aluminum

oxide (alumina) and silicon nitride, column 3 lines 25-35. At the time of the invention was made; it would have been obvious to one of ordinary skill in the art to use the SiN interposer materials teaching of Thompson to replace the alumina interposer of Bertin, because such material replacement would have been considered a mere substitution of art-recognized equivalent values, MPEP 2144.06.

Regarding claims 11, 22, Bertin discloses the intermediate board wherein said inorganic insulating material 102 is ceramic, column 3 line 15, and said conductive metal 110 a-n is copper, column 3 line 30.

But Bertin does not discloses the conductive is at least one refractory metal selected from tungsten, molybdenum, tantalum, and niobium.

However, Bertin (6,222,276 or 09/056,277 incorporated by reference as disclosed in 6255899 column 3 line 38) discloses the conductor material may consist of metals such as copper, aluminum, palladium, tungsten, or similar, column 3 line 17- 20. At the time of the invention was made; it would have been obvious to one of ordinary skill in the art to use the metal material teaching of Bertin (6,222,276) as claimed, because such material replacement would have been considered a mere substitution of art-recognized equivalent values, MPEP 2144.06.

Regarding claim 24, Bertin does not disclose wherein said intermediate board body 140 is made of a material, which is lower in coefficient of thermal expansion than said substrate board.

But Bertin discloses the intermediate board with a semiconductor device wherein said intermediate board body 140 is made of a material, which is similar to that of said substrate board including ceramic, an epoxy-glass or a glass-ceramic material, silicon or silicon-on-insulator), column 4 line 62-66 that have different coefficient thermal expansion values, column 3 lines 15-19. At the time the invention was made; it would have been obvious to one of ordinary skill in the art to use the intermediate board body and substrate board material teaching of Bertin as claimed for an intended purpose, MPEP 2144.07.

8. Claims 8 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 6255899 to Bertin et al. in view of US 6756685 to Tao.

Regarding claims 8 and 19, Bertin does not disclose the intermediate board wherein at least one side of said semiconductor device is 10 mm.

However, Tao discloses a packaging comprises a semiconductor chip having side length of 5mm, 7mm, 10mm, 13 mm, 15 mm, 20 mm and 22 mm. At the time the invention was made; it would have been obvious to one of ordinary skill in the art to use the IC size teaching of Tao with Bertin's device for making a different size semiconductor device for an intended purpose.

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thao X. Le whose telephone number is (571) 272-1708. The examiner can normally be reached on M-F from 8:00 AM - 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael M. Fahmy can be reached on (571) 272 -1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Thao X. Le
Patent Examiner
22 July 2005